REMARKS

Applicants appreciate the courtesy of Examiner Tran conducting a telephone interview with Applicants' representative on February 17, 2006. During the interview, Applicants' representative explained differences between the Applicants' claimed invention and the cited references. In a subsequent telephone conversation on February 27, 2006, Examiner Tran indicated a draft supplemental amendment of February 24, 2006 would overcome the prior art. The supplemental amendment provided herein includes identical claim amendments.

Claims 1-3, 18-21, 37-53, and 58-64 are pending in the subject application. Claims 37-53 and 58-64 were withdrawn from consideration as being directed to non-elected subject matter. Claim 1 has been amended by the present amendment. The amendment is fully supported by the application as originally filed (see, e.g., page 11, line 12 to page 12, line 3; page 86, lines 7-19; and page 90, lines 11-24; see also FIG. 2).

As amended, claim 1 recites a first input terminal into which the pulse signal is inputted, the pulse signal being inputted from the first input terminal to a gate electrode of a first transistor (see specification at page 86, lines 7-8); a second input terminal into which the clock signal is inputted, the clock signal being inputted from the second input terminal to a gate electrode of a second transistor (see specification at page 86, lines 9-10); and an output terminal from which a synchronized pulse signal is outputted (see specification at page 11, line 12 to page 12, line 3), where the clock signal has an amplitude smaller than an amplitude of the pulse signal to reduce power consumption (see page 90, lines 11-24).

Claims 1-3 and 18-20 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,894,296 to Mackawa (hereinafter "Maekawa '296") in view of U.S. Patent 5,646,642 to Maekawa et al. (hereinafter "Maekawa '642"). This rejection is respectfully traversed.

The Maekawa '296 and Mackawa '642 references, whether taken alone or in combination, do not teach or suggest a latch circuit for use in a liquid crystal display device, including at least a first input terminal into which a pulse signal is inputted, the pulse signal being inputted from the first input terminal to a gate electrode of a first transistor; a second input terminal into which a clock signal is inputted, the clock signal being inputted from a second input terminal to a gate electrode of a second transistor; and an output terminal from which a synchronized pulse signal is outputted, where the clock signal has a smaller amplitude than the pulse signal to reduce power consumption.

For example, in the Maekawa '296 reference, the clock signals CK1 and CK2 are not "inputted from the second input terminal to a gate electrode of a second transistor," as recited in claim 1. See FIG. 3 of Maekawa '296, showing the clock signals CK1 and CK2, and column 6, lines 53-58. Moreover, Mackawa '296 does not teach or suggest a latch circuit for reducing power consumption, as recited in claim 1.

On page 7 of the Office Action of 08/31/2005, it was admitted that Maekawa '296 does not teach or suggest the use of a clock signal having an amplitude smaller than an amplitude of the pulse signal, or a clock signal input control section which inputs and stops the supplied clock signal.

Applicants' comments from the Amendment filed on January 31, 2006 are incorporated by reference herein.

As discussed in the previous Amendment, the circuit disclosed in FIG. 1 of Mackawa '642 has only input terminals for the clock signals CK1, CK2, and does not teach or suggest a "second input terminal" for receiving a pulse signal, as recited in claim 1.

Consequently, the output signal Vout shown in FIGS. 1 and 2 of Maekawa '642 is merely the clock signal CK1 in the same phase amplified nearly to the level of supply voltage VDD (see column 5, lines 64-66), which does not correspond to the Applicants' claimed "synchronized

output pulse" outputted from an output terminal, as recited in claim 1. Although the output signal Vout has a larger amplitude than the clock signal CK1, it is not derived from a pulse signal, as recited in claim 1.

For at least the reasons discussed above, the Maekawa '642 reference could not be combined with Maekawa '296 to somehow produce the Applicants' claimed invention, as recited in claim 1.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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